

Quad-Channel Digital Isolators High Speed CE8640-G Series

Features:

- Compliance Halogens Free
(Br < 900 ppm, Cl < 900 ppm, Br+Cl < 1500 ppm)
- Rail-to-rail output voltage
- Guaranteed performance from -55 to 125°C
- Isolation barrier life: >60 years
- High isolation voltage between input and output (Viso=5000 V rms)

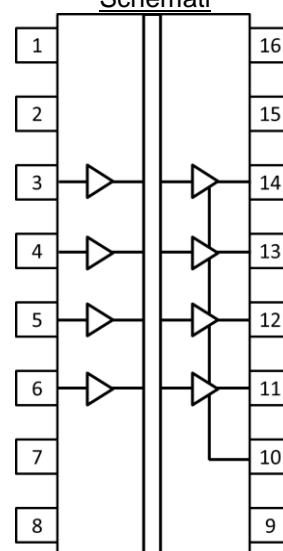
Description

The CE8640 are quad-channel digital isolators. The data rate of the CE8640 is up to 150Mbps, and the common-mode transient immunity (CMTI) is up to 200kV/us. The CE8640 provides digital channel direction configuration and the default output level configuration when the input power is lost. Wide supply voltage of the CE8640 device supports to connect with most digital interface directly, easy to do the level shift.

Applications

- Industrial automation system
- Isolated SPI, RS232, RS485
- General-purpose multichannel isolation
- Motor control

Schemati



Pin Configuration

- 1, VDD1
- 2, GND1
- 3, Input A
- 4, Input B
- 5, Input C
- 6, Input D
- 7, No Connection
- 8, GND1
- 9, GND2
- 10, No Connection
- 11, Output D
- 12, Output C
- 13, Output B
- 14, Output A
- 15, GND2
- 16, VDD2

Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{DD1}, V_{DD2}	6.5	V
Maximum Input Voltage	V_{IN}	$V_{DD}+0.4$	V
Maximum Output Voltage	V_{OUT}	$V_{DD}+0.4$	V
Output Current	I_o	15	mA
Isolation Voltage *2	V_{ISO}	5000	V rms
Operating Temperature	T_{OPR}	-55 ~ +125	°C
Storage Temperature	T_{STG}	-55 ~ +150	°C
Soldering Temperature *3	T_{SOL}	260	°C

Notes:

*1 Pulse width $\leq 1\mu s$, 300pps.

*2 AC for 1 minute, R.H.= 40 ~ 60% R.H. In this test, pins 1 to 8 are shorted together, and pins 9 to 16 are shorted together.

*3 For 10 seconds.

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{DD1}, V_{DD2}	2.5	5.5	V
High Level Input Voltage	V_{IH}	2		V
Low Level Input Voltage	V_{IL}		0.8	V

Electro-Optical Characteristics

Parameter	Symbol	Min	Typ.	Max.	Unit	Condition
Power on Reset	V_{DDPOR}		2.2		V	POR threshold as during power-up
	V_{DDHYS}		0.1		V	POR threshold Hysteresis
Input Threshold	V_{IT}		1.65		V	Input Threshold at rising edge
	V_{IT_HYS}		0.44		V	Input Threshold Hysteresis
High Level Input Voltage	V_{IH}	2			V	$V_{DD1}=5V, V_{DD2}=5V$ $V_{IN}=5V, I_o=0mA$
Low Level Input Voltage	V_{IL}			0.8	V	$V_{DD1}=5V, V_{DD2}=5V$ $V_{IN}=5V, I_o=0mA$
High Level Output Voltage	V_{OH}	$V_{DD}-0.4$			V	$I_{OH} = -4mA$
Low Level Output Voltage	V_{OL}			0.4	V	$I_{OL} = 4mA$
Output Impedance	R_{out}		50		Ω	
Supply Current	$I_{DD1}(Q0)$			2.04	mA	$V_{DD1}= 5V$ All Input 0V
	$I_{DD2}(Q0)$			4.84	mA	$V_{DD2}= 5V$ All Input 0V
	$I_{DD1}(Q1)$			8.68	mA	$V_{DD1}= 5V$ All Input at supply
	$I_{DD2}(Q1)$			4.98	mA	$V_{DD2}= 5V$ All Input at supply
	$I_{DD1}(1M)$			5.1	mA	$V_{DD1}= 5V$ All Input with 1Mbps
	$I_{DD2}(1M)$			4.39	mA	$V_{DD2}= 5V$ All Input with 1Mbps
	$I_{DD1}(10M)$			5.34	mA	$V_{DD1}= 5V$ All Input with 10Mbps
	$I_{DD2}(10M)$			6.68	mA	$V_{DD2}= 5V$ All Input with 10Mbps
	$I_{DD1}(100M)$			7.47	mA	$V_{DD1}= 5V$ All Input with 100Mbps

Supply Current	$I_{DD2}(100M)$	38.12	mA	$V_{DD2}=5V$ All Input with 100Mbps
	$I_{DD1}(Q0)$	1.96	mA	$V_{DD1}=3.3V$ All Input 0V
	$I_{DD2}(Q0)$	4.74	mA	$V_{DD2}=3.3V$ All Input 0V
	$I_{DD1}(Q1)$	8.59	mA	$V_{DD1}=3.3V$ All Input at supply
	$I_{DD2}(Q2)$	4.86	mA	$V_{DD2}=3.3V$ All Input at supply
	$I_{DD1}(1M)$	4.98	mA	$V_{DD1}=3.3V$ All Input with 1Mbps
	$I_{DD2}(1M)$	4.22	mA	$V_{DD2}=3.3V$ All Input with 1Mbps
	$I_{DD1}(10M)$	5.13	mA	$V_{DD1}=3.3V$ All Input with 10Mbps
	$I_{DD2}(10M)$	5.72	mA	$V_{DD2}=3.3V$ All Input with 10Mbps
	$I_{DD1}(100M)$	6.6	mA	$V_{DD1}=3.3V$ All Input with 100Mbps
	$I_{DD2}(100M)$	25.73	mA	$V_{DD2}=3.3V$ All Input with 100Mbps

Parameter	Symbol	Min	Typ.	Max.	Unit	Condition
Propagation Delay	t_{PLH}	2.5	9	15	nS	$V_{DD1}=5V, V_{DD2}=5V$
	t_{PHL}	2.5	11	15	nS	
Pulse Width Distortion	PWD			5	nS	
Rising Time	T_r		2.3	5	nS	
Falling Time	T_f		2	5	nS	
Channel-to-Channel Delay Skew	$t_{SK}(c2c)$			3	nS	
Disable high to Tri-State	t_{PHZ}			30	nS	
Disable low to Tri-State	t_{PZH}			30	nS	

Disable low to Tri-State	t _{PLZ}			30	nS
Enable to Data high Valid	t _{PZL}			30	nS
Common Mode Transient Immunity	CMTI	±200	-	-	kV/μS

Order Information

Part Number

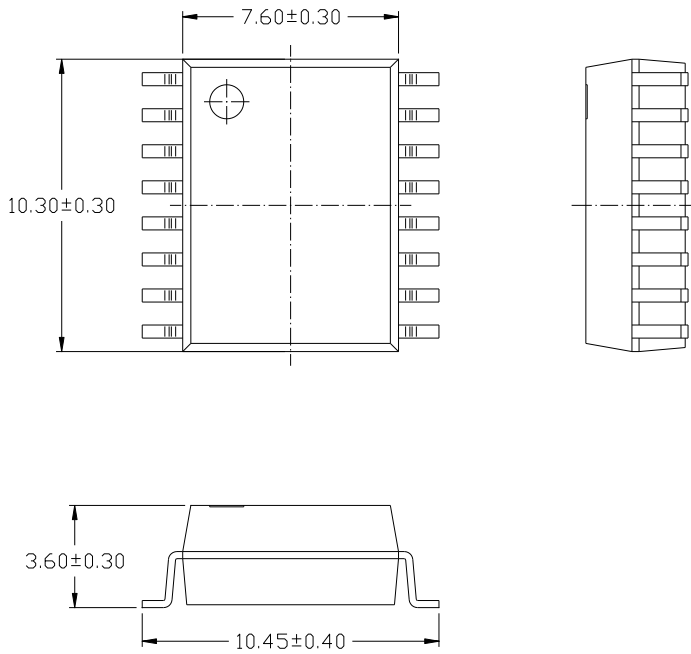
CE8640(X)-VG

Note

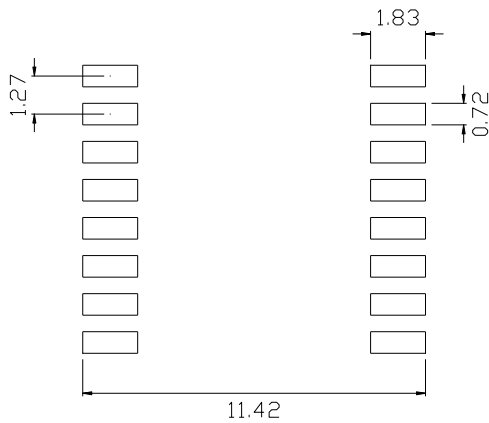
CE = denotes EVERLIGHT
8640 = part no.
X = Tape and reel option (TA, TB)
V = VDE (optional)
G = Halogens free

Option	Description	Packing quantity
(TA)	Surface mount lead form + TA tape & reel option	850 units per reel
(TB)	Surface mount lead form + TB tape & reel option	850 units per reel

Package Dimension
(Dimensions in mm)

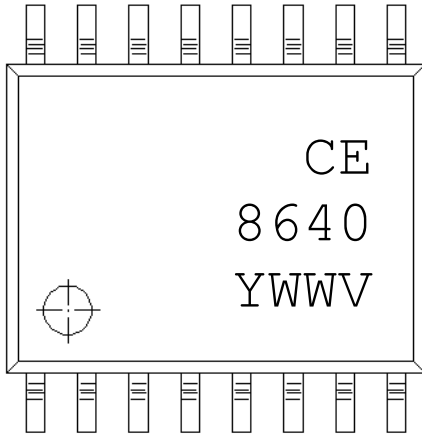


Recommended pad layout for surface mount leadform



Notes.
Suggested pad dimension is just for reference only.
Please modify the pad dimension based on individual need.

Device Marking



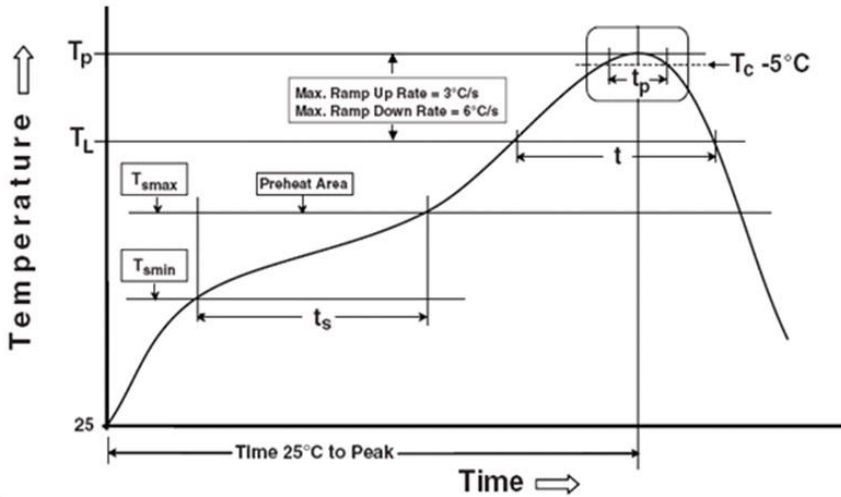
Notes

CE	denotes EVERLIGHT
8640	denotes Device Number
Y	denotes 1 digit Year code
WW	denotes 2 digit Week code
V	denotes VDE (optional)

Precautions for Use

1. Soldering Condition

1.1 (A) Maximum Body Case Temperature Profile for evaluation of Reflow Profile



Note:

Reference: IPC/JEDEC J-STD-020D

Preheat

Temperature min (T_{smin})	150 °C
Temperature max (T_{smax})	200°C
Time (T_{smin} to T_{smax}) (t_s)	60-120 seconds
Average ramp-up rate (T_{smax} to T_p)	3 °C/second max

Other

Liquidus Temperature (T_L)	217 °C
Time above Liquidus Temperature (t_L)	60-100 sec
Peak Temperature (T_P)	260°C
Time within 5 °C of Actual Peak Temperature: $T_P - 5^\circ\text{C}$	30 s
Ramp- Down Rate from Peak Temperature	6°C /second max.
Time 25°C to peak temperature	8 minutes max.
Reflow times	3 times

DISCLAIMER

1. Above specification may be changed without notice. EVERLIGHT will reserve authority on material change for above specification.
2. The graphs shown in this datasheet are representing typical data only and do not show guaranteed values.
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